UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,470	01/26/2005	Roeland John Heijna	NL 020697	3646

65913 7590 08/08/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
HUANG, DAVID S	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
08/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/522,470	HEIJNA, ROELAND JOHN	
	Examiner	Art Unit	
	DAVID HUANG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,7 and 11-14* is/are allowed.

6)☒ Claim(s) *1 and 3-6* is/are rejected.

7)☒ Claim(s) *8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, with respect to claims 1 and 3 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of King et al. (US 6,657,488).

2. Applicant's arguments with respect to claims 4 and 5 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, with respect to the declaration have been fully considered and are persuasive. The objection to the declaration has been withdrawn.

4. Applicant's arguments, with respect to section headings in the specification have been fully considered and are persuasive. The objection to the specification has been withdrawn.

5. Applicant's arguments, with respect to claims 4-9 have been fully considered and are persuasive. The objection to claims 4-9 has been withdrawn.

6. Applicant's arguments, with respect to claims 8-10 have been fully considered and are persuasive. The 112, 2nd paragraph rejection to claims 8-10 has been withdrawn.

Claim Objections

7. **Claims 1 and 3** are objected to because of the following informalities:

Claim 1 has been amended to remove all the reference characters in the claims, but line 6, retains the reference character "(B)". This should be removed to improve consistency in the claims.

Claim 3 is dependent on claim 1, and contains the same defects.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,377,633) in view of King et al (US 6,657,488).

Regarding **claim 1**, Schneider discloses a method of setting a slice level in a binary signal in presence of noise, the binary signal having a first signal level during a first signal portion and a second signal level during a second signal portion, the method comprising the steps of:

setting the slice level initially at a level intermediate the first and the second (B) signal level (column 7, lines 8-14),

providing a noise indication by measuring a first peak level (positive peak register, column 3, lines 45-50) during the first signal portion (column 3, lines 58-61), and

adjusting the slice level using the noise indication (column 3, lines 62-65),

characterized in that

the step of providing a noise indication includes measuring a second noise level during the second signal portion (negative peak register, column 3, lines 45-50), and in that

the step of adjusting the slice level includes adjusting the slice level substantially uniformly during both the first and the second signal portions (threshold signal value used to

determine the mid-bit reference; column 3, lines 58-65; the same adjusted mid-bit reference is used to distinguish between both binary zero and one).

However, Schneider fails to expressly disclose measuring noise levels of a binary signal and adjusting the slice level based on the measured noise levels.

King et al. teaches providing an adjustable slicing level to compensate for the asymmetric noise characteristic by introducing an offset to create the most reliable output in creating a more symmetric margin and optimize noise margin. This is implemented by using a closed-loop approach to dynamically adjust the slicing voltage (column 2, line 64 - column 3, line 22, Fig. 2A). Thus, it is implicit that a slicing offset is generated based on asymmetry due to some magnitude of noise current.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Schneider with the slicing level adjusting teaching of King et al. since it improves performance by providing a more symmetric slicing margin and better results by optimizing noise margin and signal strength (column 3, lines 12-15).

Regarding **claim 3**, Schneider discloses everything claimed as applied to claim 1 above, and further discloses measuring the respective noise levels involves detecting peaks in the binary signal (Negative and positive peak registers, column 3, lines 45-50; see also Figure 4, registers 56 and 58).

10. **Claims 4 and 5** rejected under 35 U.S.C. 103(a) as being unpatentable over Nagaraj (US 6,041,084).

Regarding **claim 4**, Nagaraj discloses a device for setting the slice level in a binary signal in the presence of noise, comprising:

a first level shifter (VOS 18, Figure 4) coupled between a pair of input terminals (V_{OP} and V_{ON}, Figure 4) for receiving the binary signal (V_{OP} and V_{ON}, column 3, lines 57-59, Figure 4) and a pair of output terminals (V_{OP2}, V_{ON2}, Figure 4) for supplying and adjusted binary signal,

a second level shifter coupled to the pair of input terminals (V_{OS} 18, Figure 4, also interpreted to be the "second" level shift means, since it also provides shifted input signals to the noise peak detection below),

a noise peak level detection unit (20H and 20L, Figure 4) that receives shifted input signals and producing a noise indication signal (offset voltage VOS, column 3, line 65 - column 4, line 4, Figure 4) indicative of any difference in noise levels between signal portions of the binary signal having different signal levels, the noise peak level detection unit coupled to the second level shifter (Fig. 4), and

an adjustment connection for feeding the noise indication signal to both the first and the second level shifters so as to compensate for any difference in the noise levels (column 4, lines 2-8, Integration 28, Figure 4).

However, Nagaraj fails to expressly disclose wherein the first shifter subtracts the noise indication signal from the signal levels of the binary signal to produce the shifted input signals.

Nevertheless, Nagaraj teaches that offset voltages are opposite polarity so that V_{OS} adds to V_{ON} and subtracts from V_{OP}. In reference to Figs. 5D and 5E, the absolute value of each of the differential binary signals is reduced, and moved towards zero. Thus, it is implicit that V_{OS} is subtracted from the value of the binary signals.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to specify the first shifter subtracts the noise indication signal from the

signal levels of the binary signal, since it is implicitly taught by Nagaraj that by applying offset voltages of opposite pluralities, the absolute value of each signal is subtracted by the offset value.

Regarding **claim 5**, Nagaraj discloses everything claimed as applied to claim 4 above, and further discloses the noise peak level detection unit includes a first peak detector for detecting peaks in a first signal level of the binary signal and supplying a first peak detection signal (Positive Peak Det 20H and V_{P1}, Figure 4), a second peak level detector for detecting peaks in a second signal level of the binary signal and supplying a second peak detection signal (Negative Peak Det 20L and V_{P2}, Figure 4), and a differential amplifier for amplifying a difference between the first and the second peak detection signals to produce the noise indication signal (AND 26, column 3, line 65 - column 4, line 2, Figure 4).

11. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagaraj (US 6,041,084) in view of Bradbeer (US 5,130,543)

Regarding **claim 6**, Nagaraj discloses everything claimed as applied to claim 4 above, but fails to expressly disclose the adjustment connection includes a low-pass filter for filtering the noise indication signal.

Nevertheless, Nagaraj does disclose the output of the differential amplifier 26, is integrated by an integrator circuit.

It is well known in the art that integrators are implemented as low pass filters as evidenced by Bradbeer (column 18, line 68 - column 19, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specify the integrator circuit taught by Nagaraj to be a low pass filter as claimed because low pass filters are well known in the art to be used as integrators.

Allowable Subject Matter

1. **Claims 2, 7, and 11-14** are allowed.

2. **Claims 8-10** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a statement of reasons for the indication of allowable subject matter: The present invention for adjusting a slice level in a binary signal in the presence of noise comprises method steps for setting the slice level initially at a level intermediate the first and second signal levels, providing a noise indication, adjusting the slice level. The closest prior art, Schneider (US 6,377,633), teaches a similar method that also sets the slice level at the midpoint between two signal level, provides peak detection, and adjusts the slice level using the peak detection. However, the closest prior art fails to disclose specifically that the slice level is set at a value substantially equal to half the difference between the magnitudes of the first (A) and the second (B) signal levels minus half the difference between the magnitudes of the first and second noise level. This limitation distinguishes claim 2 over the prior art.

The present invention also discloses a device for setting the slice level in a binary signal in the presence of noise with first and second shift means, a noise peak level detection means and an adjustment connection. The closest prior art, Nagaraj (US 6,041,084), teaches a similar device with variable voltage offset voltage sources, peak detectors, a differential amplifier, and a

feedback integrator. However, Nagaraj fails to disclose that the shifting means comprise a series connection of a resistive element, a transistor, and a current source, wherein the bases of the transistors being coupled to receive the noise indication signal (as recited in claim 7). Nagaraj also fails to disclose the noise peak level detection means comprise a RMS level detector and the first and second differential amplifiers for supplying level compensated noise signals to the peak detectors (as recited in claims 8 and 10). These limitations distinguish claims 7, 8 and 10-14 over the prior art.

Citation of Pertinent Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stratton (US 4,707,740) discloses adjusting slice level as a function of noise measured.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID HUANG whose telephone number is (571)270-1798. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSH/dsh
8/4/2008
/David Huang/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611